REMARKS

Claims 1 and 3-10 are pending in the above-identified application. Claim 2 has been canceled. Claims 1, 3, 4, 9, and 10 have been elected for prosecution on the merits. Claim 1 is independent.

Entry of the Amendment is Proper

Claim 1 has been amended to correct a typographical error in the clean copy of the claim, as well as to clarify the meaning of "layers formed at the same time in self-alignment." Entry of the amendment is proper because the amendment at least places the application in better form for appeal.

Drawings

Figures 5 and 6 have been objected to for not being designated "Prior Art." Accordingly, Applicants provide herewith corrected formal drawings for Figures 5 and 6.

Claim Rejection – 35 U.S.C. 112

Claim 1 has been rejected under 35 U.S.C. 112, second paragraph, as being indefinite, due to the phrase "is made of a silicide layer" found in claim 1's clean copy. Applicants note that the phrase had been canceled in the marked-up version of the claim. Apparently the phrase remained in the clean copy of the claim. Thus, the claim has been amended to remove the phrase.

Claim Rejection – 35 U.S.C. 102(b)

Claims 1-3 have been rejected under 35 U.S.C. 102(b) as being anticipated by Horiuchi et al. (IEEE, hereinafter Horiuchi). Applicants respectfully traverse this rejection.

The Office Action states that, "the limitation that both of the silicide layers are formed at the

same time in self-alignment is not given any patentable weight because this is product by process language and will not change the final structure that is being claimed." Applicants submit that it is not true that the so-called product by process limitation will not change the final structure.

In Horiuchi et al. the silicide layer on the source/drain regions and a silicide layer on a gate electrode are formed of different materials, and the MOSFET does not include a silicide layer. Thus, the silicide layer on the source/drain regions and silicide layer on a gate electrode, as well as a comparable layer on the MOSFET could not have been formed at the same time in self-alignment.

In the present specification, titanium silicide layers 7 are formed by Saliside on source/drain regions and the gate electrodes of the MOSFET, as well as on anodes and cathodes in the Schottky barrier diode (Specification: page 9, first full paragraph).

In order to emphasize this difference, Applicants have amended claim 1 to include that the silicide layers are formed of the same materials, as follows:

"..., and both of the silicide layers are layers formed at the same time in self-alignment **of the same materials**."

Further with respect to claim 3, Applicants submit that because Horiuchi does not teach silicide layers formed of the same materials, it also does not teach layers formed of the specific materials of claim 3.

Accordingly, Applicants submit that Horiuchi fails to teach each and every claimed element. Applicants respectfully request that the rejection be withdrawn.

Claim Rejection – 35 U.S.C. 103; Horiuchi and Iwata

Claim 4 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Horiuchi in view

of Iwata et al (U.S. Patent 6,255,704, hereinafter Iwata). Applicants respectfully traverse this rejection.

Iwata is relied on for teaching converting a titanium silicide layer to a C54 crystalline structure. However, because Horiuchi does not teach silicide layers formed of the same materials, it also does not teach layers formed of the specific materials of claim 4. Accordingly, Applicants submit that the Horiuchi and Iwata, either alone or in combination, fail to teach each and every claimed element. Applicants respectfully request that the rejection be withdrawn.

Claim Rejection – 35 U.S.C. 103; Horiuchi and Tuttle

Claims 9 and 10 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Horiuchi in view of Tuttle (U.S. Patent 6,122,494). Applicants respectfully traverse this rejection.

Tuttle is relied on for teaching the claimed IC module or IC card. However, Tuttle also does not disclose a Schottky barrier diode and a MOS transistor formed on a single substrate, and thus does not make up for the above stated deficiencies in Horiuchi. Thus, at least for this reason, the rejection fails to establish *prima facie* obviousness. Accordingly, Applicants respectfully request that the rejections be withdrawn.

CONCLUSION

In view of the above amendments and remarks, reconsideration of the various rejections and allowance of claims 1 and 3-10 is respectfully requested.

Should the Examiner have any questions concerning this application, the Examiner is invited to contact Robert W. Downs (Reg. No. 48,222) at (703) 205-8000 in the Washington, D.C. area.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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Attachment:

Replacement Sheet (Figures 5 and 6)